X2000 Bus Selection and Evolution of Bus Architecture

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The X2000 Program

- A NASA funded advanced technology program which enables low cost science missions

- X2000 Vision Statement:

  Develop environmentally immune, high performance, low power low mass, low cost, mass reproducible core electronics, which can be used in a plug and play mode, not unlike a PC, compatible with JPL's Mission Data System (MDS) software for multiple missions

- Multiple deliveries:
  - First Delivery
    - Targeted for the OP/SP (Pluto/Kuiper Express & Europa Orbiter) missions
    - Development is in progress
  - Future deliveries are under study

X2000 System Bus Major Requirements

- Advanced technology (X2000 is a technology program)
- Multi-mission
- Low cost
- High performance
- Low power, mass, and volume
- Reliable and fault tolerant

Other Bus Selection Criteria

- Prefer Commercial Standard Interfaces
  - Low cost
    - Low development cost due to reusable designs
    - Reduced recurring cost due to large market demands
    - Lower test & integration cost due to widespread usage and low cost test equipment
  - Avaliability
    - Space qualified parts are more difficult to find nowadays
    - Available Intellectual Property (IP)
    - Available commerical software (OS, software drivers)
  - Performance
    - Performance of commercial standards usually lead space qualified parts
  - Reliability Issue
    - Commercial standards have limited fault tolerance
    - Need to be compensated by system level design

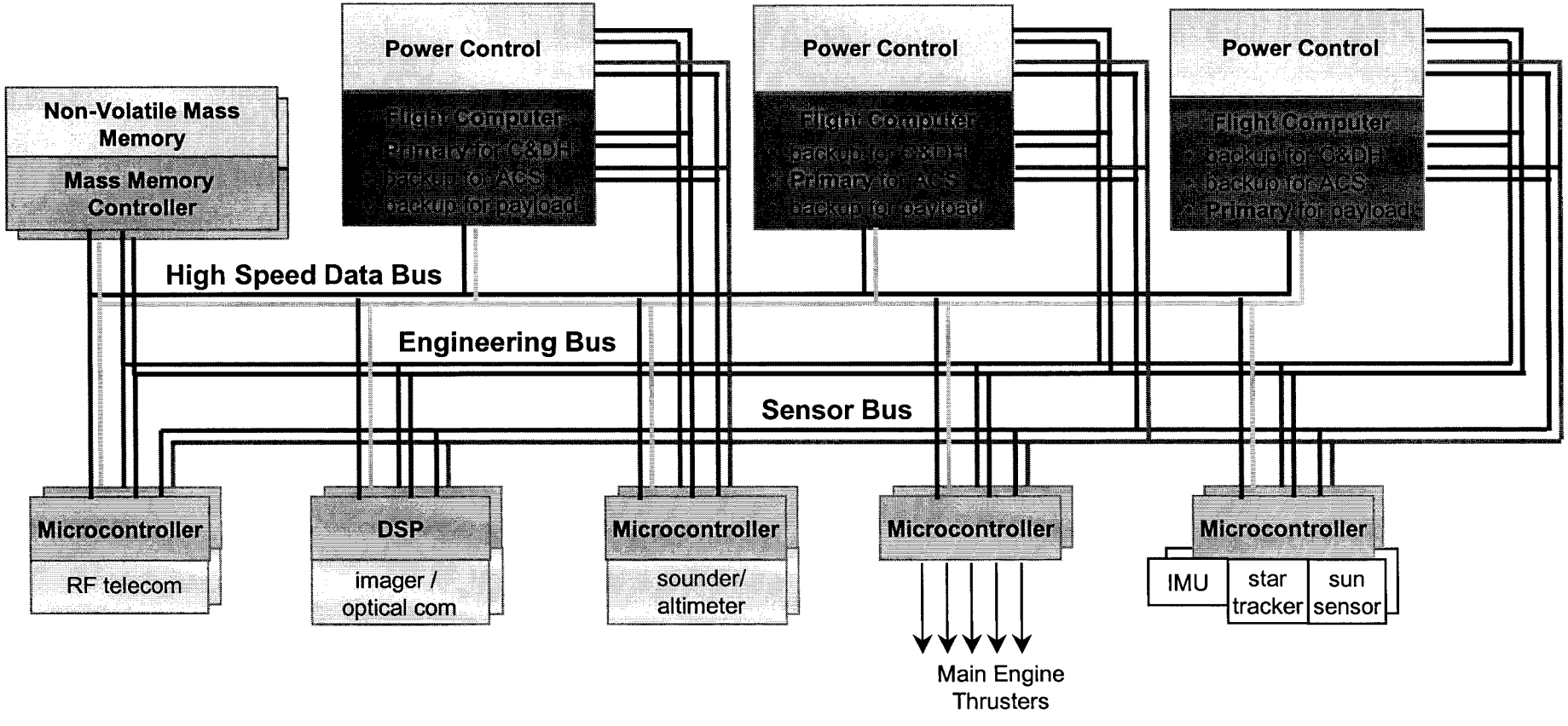
X2000 System Bus Architecture Design Strategy

- To meet both high performance and low power requirements, a multi-level bus architecture was conceived
  - High speed data bus
  - Medium speed and moderate power engineering bus
  - Low power sensor bus
- To achieve the multi-mission objective, the system bus must be
  - Scalable
  - Distributed
  - Symmetric

  This lends itself to multi-master bus architectures
- Redundant buses in each level will be used for fault tolerance

Initial X2000 Avionics System Architecture Concept

Jan 1997



High Speed Data Bus

- **Functions**
  - Transfer High Speed Science Data
  - Facilitate Transaction of Time Critical Messages (e.g., Uplink commands)
  - Support Optical Communication
  - Fast Memory Load
- **Desired Characteristics**
  - Data Rate >= 100 Mbps
    - Technology Roadmap
    - Europa Orbiter imaging data requries 40 Mbps
  - Power < 1.5 W/node
  - Multi-Master for scalability
  - Support Priority Arbitration for Timely Delivery of Critical Messages
  - Commercial Standard
  - Relatively Low Complexity
  - ASIC Core Available
  - Fault Tolerant
  - Compatible with MCM stack configuration

Engineering Bus

- **Functions**
  - Transfer commands and engineering data for
    - Attitude Control
    - Thruster Control
    - Power Switching
    - RF Communication
- **Desired Characteristics**
  - Data Rate ≈1 Mbps
  - Power < 0.5 W/node
  - Multi-Master for scalability
  - Support Priority Arbitration for Timely Delivery of Critical Messages
  - Commercial Standard
  - Relatively Low Complexity
  - ASIC Core Available
  - Fault Tolerant
  - Compatible with MCM stack configuration

Eliminated from X2000 architecture due to marginal power benefit but significant complexity

Sensor Bus

- **Functions**
  - Collect telemetry data from temperature, current, voltage, and pressure sensors
- **Desired Characteristics**
  - Data Rate ≈ 10 kbps
  - Power < 0.01 W/node
  - Multi-Master for scalability
  - Support very simple sensor interface
  - Commercial Standard
  - Low Complexity
  - ASIC Core Available
  - Fault Tolerant
  - Compatible with MCM stack configuration

Later on incorporated some Engineering bus functions and became the Low Power Engineering Bus

System Buses Selection Process

Step 1: Literature and web search of available standard buses in the industry

Step 2: Consulted with in-house and industry experts (e.g., ATM, 1773)

Step 3: Established a set of selection criteria with X2000 Program Managers

Step 4: Hosted an X2000 Interface Workshop and invited speakers from the industry and JPL. Also collected information with questionnaires based on selection criteria.

Step 5: The design team evaluated the buses with the selection criteria.

Step 6: Held the first bus selection meeting. Participants included engineers from the previous projects. A primary candidate and a backup candidate were selected for further study for the high speed data bus, the engineering bus, and the low power sensor bus.

Step 7: More detailed evaluation of the primary and secondary candidates

Step 8: Held the second bus selection meeting. Only one candidate was selected for each bus

Step 9: Re-evaluated the 3-bus architecture and decided the engineering bus has only marginal benefits but would add significant cost and complexity. A 2-bus architecture was then adopted.

Summary of Standard Interface Survey

Bus Name	Type	Power/interface	Speed	Multi-master	Topology	Source of Standard	Organization Involved
IEEE 1394 (cable)	serial	1.1 W / 0.5 W	100, 200, 400 Mbps	Yes	Tree	IEEE 1394-1995	Adaptec, Apple, Skipstone, TI
IEEE 1394 (backplane)	serial	2.1 W/ 1.1 W	25 Mbps, 50 Mbps	Yes	Multi-Drop Bus	IEEE 1394-1995	LMFS, APL
Fibre Channel	serial	3 W	133 Mbps to 2 Gbps	Yes	pt-to-pt, loop, star	ANSI X3T11	Ancor, Hewlett Packard, and IBM
1773A	serial	1.6 W/ 0.9 W	1 Mbps or 20 Mbps	cmd-rsp*	Star	SAE AS 1773	Honeywell, SCI, Boeing, UTMC
Fast Ethernet	serial	1.9 W	100 Mbps	Yes	Multi-Drop Bus	IEEE 802.3	Numerous companies
ATM	netwk	10 W	155 Mbps to 622 Mbps	Yes	network	ATM Forum	> 220 companies
SFODB	serial	5 W	1 Gbps	Yes	ring	adopted by IEEE p1393	Boeing, GSFC, OAI
PFODB	parall	5 W	1.5 Gbps	Yes	ring	Optivision	GSFC, Optivision
Myrinet	parall	11 W/8-port switch	1.28 Mbps/connection	one-to-one	cross-bar switch	Myricom	Myricom
Serial Coherant Interf	serial	unknown	1250 MHz	Yes	Ring	IEEE p1596	Not fully supported
FDDI	netwk	13.5 W	100 Mbps	Yes	dual ring	ANSI X3T9.5	
Low Power Serial Bus	serial	0.1 W	1 Mbps	cmd-rsp*	Multi-Drop Bus	JPL modified 1553B	UTMC, Boeing for protocol chip
CAN	serial	0.25 W	1 kps to 1 Mbps	Yes	Multi-Drop Bus	Bausch-Lomb	Auto industry companies
Ethernet	serial	0.3 W	10 Mbps	Yes	Multi-Drop Bus	IEEE 802.3	Numerous companies
SPI	serial	0.028 W	5 Mbps	one-to-one	pt-to-pt	Motorola	Motorola
Universal Serial Bus	serial	0.85 W	12 Mbps	Yes	Tree	Intel	Intel,Philips, TI
I^2C	serial	0.01 W	1.5 kps to 90 kbps	Yes	Multi-Drop Bus	Phillips	Phillips, Siemens, Intel,TI
J1850	serial	0.052 W	10.4 kbps	Yes	Multi-Drop Bus	SAE J1850	Auto industry companies
MicroLAN	serial	parasitic power	16.3 kbps	cmd-rsp*	Multi-Drop Bus	Dallas Semiconductor	Dallas Semiconductor
Access Bus	serial	0.25 W	100 kbps	Yes	Multi-Drop Bus	Phillips & DEC	over 60 companies

* command-response

Selection Summary
High Speed Data Bus

	1st Round Selection	2nd Round Selection
IEEE 1394	✓Very good data rate, moderate power, strong commercial support, relatively deterministic latency, no rad-hard parts but ASIC core available, although weak in fault-tolerance	✓Power is moderate and data rate is appropriate, tree topology can be fitted into the MCM stack by using linear tree, fault protection can be achieved by mirroring the linear tree
Fiber Channel	✓Excellent data rate, strong commercial support, flexible protocol & topology, excellent isolation, no rad-hard parts but ASIC core available, although high power and weak in fault-tolerance.	Power is too high, optical connector is not compatible with MCM stack configuration, although the flexible protocol and topology are attractive. May be applicable for 2nd delivery
Mil-Std-1773a	Data rate low for X2000, high power, not multi-master, limited commercial support, although built-in redundancy and excellent isolation	
Fast Ethernet	Not suitable for real time application due to indeterminstic bus latency, also no rad-hard parts or ASIC core, although commercial support is excellent	
ATM	Too complicate and high power, no rad-hard parts or ASIC core, although commercial support is excellent	
SFODB	Power too high and is not a real standard, although data rate and isolation are excellent	
PFODB	Power too high and is not a real standard, although data rate and isolation are excellent	
Myrinet	Power too high, not rad-hard parts or ASIC core, not a real standard, although data rate is extremely high.	
SCI	Not sufficient support from the industry, not implemented by any vendor at the time of survey	
FDDI	Too complicate and high power, no rad-hard parts or ASIC core, commercial support is giving way to ATM	

IEEE 1394 and Fibre Channel Comparison

	1394	Fibre Channel	Adavantage
Power	TI Link (TSB12C01A) = 0.74 W	10 W/node(includes proc. and mem)	IEEE 1394
	TI Phy (TSB11C01) = 0.75 W	2.5 w. core only, 0.6 W transceiver	
	Total = 1.5 W/ node		
Core Availability	LM - Flatten VHDL	Synbios verilog core OK	FC (1394 core may
	Mixed signal logic	Boeing core a probability	be available from
	Reluctant		other vendors)
Complexity	~150 k (BP, No isoc)	~ 400 k (Embed RISC need ? Symbios)	IEEE 1394
	50 k (cable, isoc -TI)	~ 60 k (no RISC, no mem - Boeing)	
Connector	Ext. to stack - 0.3 x 0.5 x 0.36	Standard SC conn - 0.5 x 0.5 x 1	IEEE 1394
	Int to stack - elestomeric	Boeing Fc ~ SC	
Isolation	Cable - needs isolation between Phy and Link	Fiber optic	FC better, both OK
	Backplane - OK		
Commercial Bd -	Adaptec (cable and S/W Dev)	Symbios (S/W dev)	
PCI + Dev tools	TI (cable + S/W development)	Adaptec (S/W dev)	Same
	Board may be different from final version	may be different from final because of implementation	
	bridge not available for backplane to cable	dependence	
Reliability	Backplane - OK	Need redundant loop	FC (slightly)
	Cable - a node fail can fail a subtree		
	may use redundant bus but more complex		
Fault Isolation	8 % overhead	25% overhead	FC more robust
			1394 less overhead
Future Expansion	Protocol fixed	Protocol flexible	FC

Selection Summary
Engineering Bus

Removed due to marginal power benefit but significant complexity

	Reason	Reason
LPSB	✓Protocol well understood, data rate is appropriate for engineering bus, much lower power than standard 1553, bus latency is controllable, ASIC core being developed by JPL, built-in redundancy, although it deviated from 1553 standard	✓Power is much lower than 1773 and electrical connection is compatible with MCM stack, its deviation from standard is small and can be accommodated by additional circuit
AS1773	✓Protocol well understood, data rate is extendable to 20 Mbps, bus latency is controllable, built-in redundancy, no deviation from standard, strong isolation, ASIC core being developed by JPL, although its power is relatively high	Power is much higher than LPSB and optical connection not compatible with MCM stack
CAN	Bus latency is too indeterministic for engineering bus, message size is small, raw bit rate is appropriate (1 Mbps) but effective bandwidth is low due to high overhead, although commercial support is strong and ASIC core is available	
Ethernet	Not suitable for real time application due to indeterminstic bus latency, also no rad-hard parts or ASIC core, although commercial support is excellent	
SPI	Not enough protocol support (need design in software), not a real bus (basically a point-to-point link)	
USB	Very similar to 1394 but much lower data rate and yet power is the same	

Selection Summary
Low Power Sensor Bus

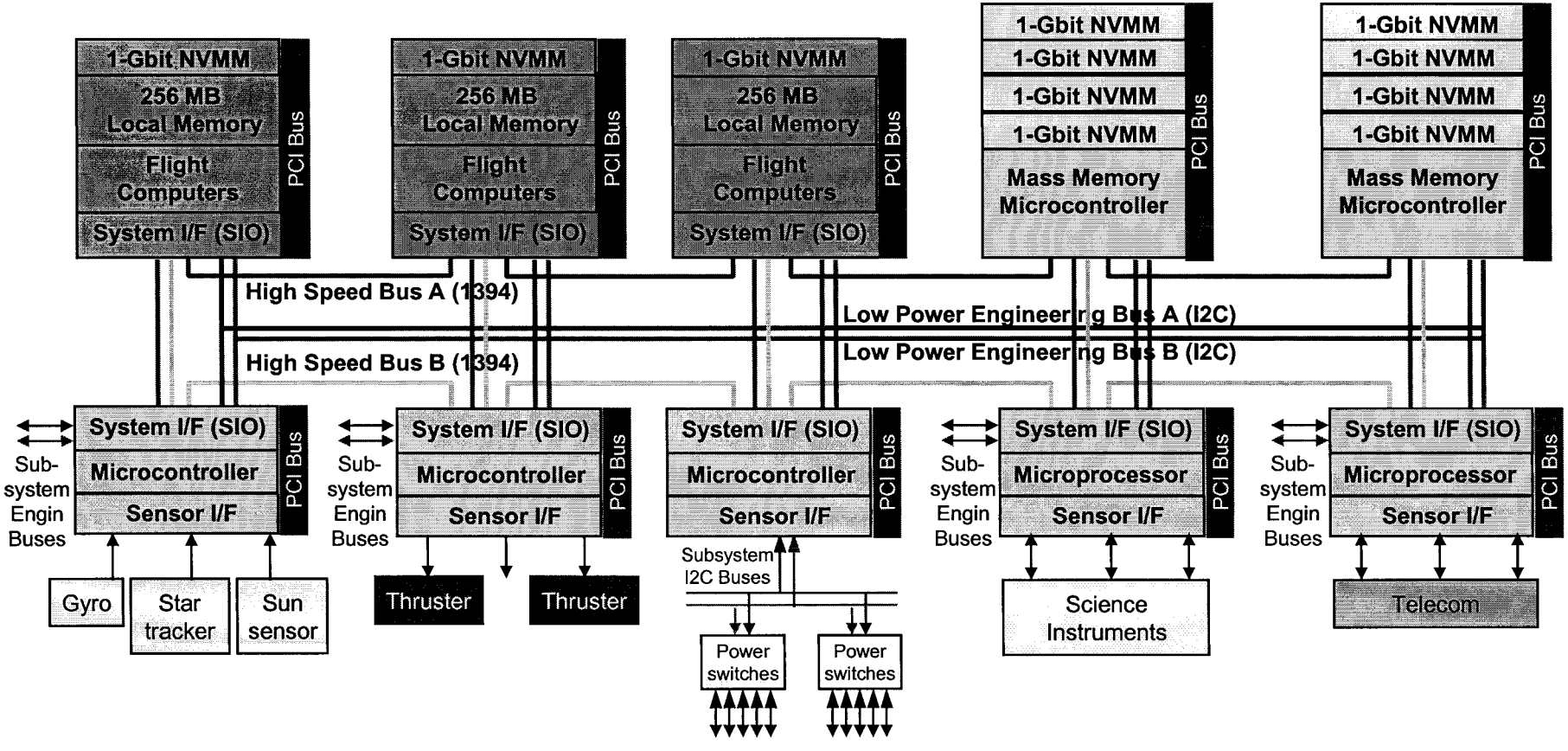
Changed to Low Power Engineering Bus

	Reason	Reason
I2C	✓Very low power, multi-master, both rad-hard parts and ASIC core available, adequate data rate (100 to 400 kbps), simple protocol, strong commercial support	✓Lower power than J1850, both rad-hard parts and ASIC core are readily available
J1850	✓Moderate power, multi-master, adequate data rate (10 kbps), protocol similar to CAN, fairly strong commercial support, it is not sure if ASIC core available	Although power is moderate, it's still significantly higher power than I2C, no rad-hard parts or ASIC core found
CAN	Power is too high for sensor bus	
MicroLan	Rad-hard part and ASIC core are not available, design not transferrable to rad-hard foundry	

*Note: After I2C is chosen to assume the role of engineering bus, its message size has to be restricted to 100 (overhead considered) in order to meet on-board relative time accuracy requirement. An important function of the engineering bus, the RTI distribution, can be accommodated by the "general call" address of the I2C.

X2000 Initial Baseline Avionics System Architecture

Nov 1997



Issues Regarding Original Baseline

- The 1394 and I2C are commercial buses not designed for high reliability applications
- Physical layer failure in any node can bring down the entire 1394 Bus
- A babbling node may keep sending bus reset signals on the 1394 bus and thus disables the bus
- The loading on I2C is likely exceeding the 400 pf specified in the standard
- The 1394 and I2C interfaces are in the same ASICs, and thus their fault containment regions are overlapped

Tiger Team Review of Bus Architecture

- To determine if the 1394 and I2C are the right buses for X2000
- To investigate techniques that may improve the reliability of the 1394 and I2C buses

Process of Tiger Team Review

- Use the Cassini 1553 Bus as the "golden standard of reliable bus" and see if the 1394 Bus can be enhanced to match that standard
- Investigate whether other buses are less complex and more reliable than the 1394 Bus.
- Investigate techniques to improve the reliability of I2C Bus to the level comparable to the Cassini 1553 Bus
- Examine several low power bus architecture options to determine if there is a better alternative to the I2C bus.

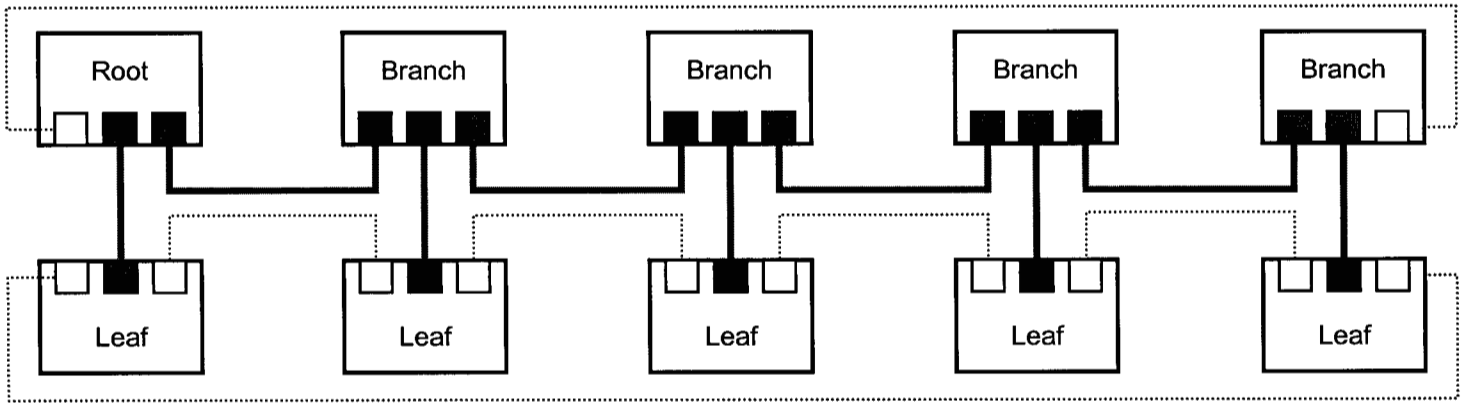
Conclusion of Tiger Team Review

- The IEEE 1394 Bus was preserved because:
  - Reliability of the IEEE1394 bus can be enhanced to a level comparable to the Cassini 1553 Bus with the port disable and reroute technique
  - Only the IEEE1394 bus can meet the prospective performance requirement of the Europa Orbiter mission
  - The power consumption of IEEE 1394 bus is moderate compare to other high speed buses
  - The multi-master capability of 1394 bus is necessary for implementing distributed system
  - The 1394 Bus has a roadmap beyond 400 Mbps. This can enable many high performance missions in the future
- The I2C Bus was also preserved with added enhancements
  - The system I2C Bus is used only to support IEEE 1394 bus recovery. Engineering data are carried by the IEEE1394 or the subsystem I2C bus
  - Add fail-silence mechanism to protect the system and subsystem I2C buses
  - Enhance I2C bus driver to cope with the required bus loading

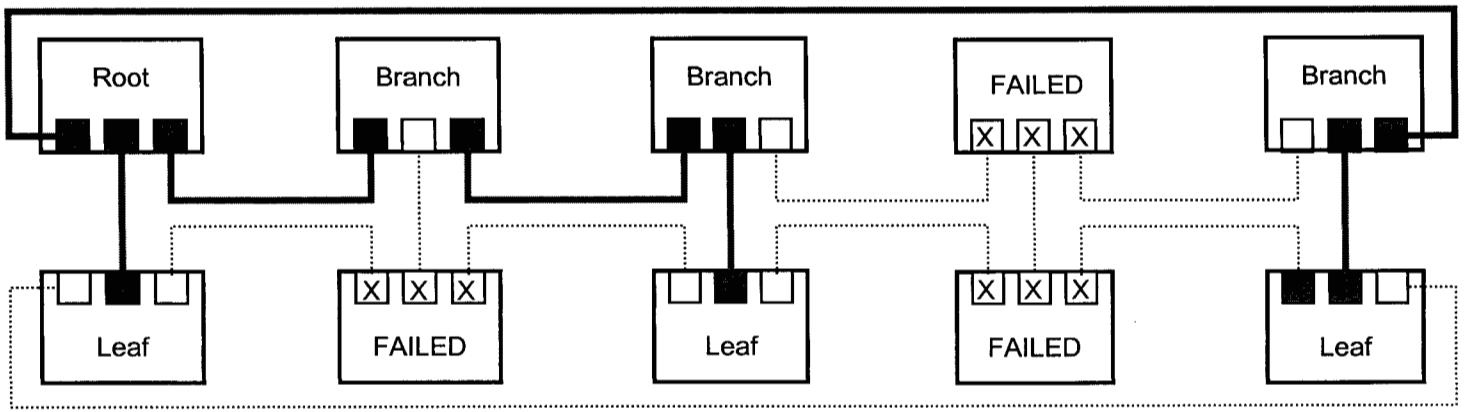
Port Disable and Reroute of 1394

- Basic Idea of the Technique

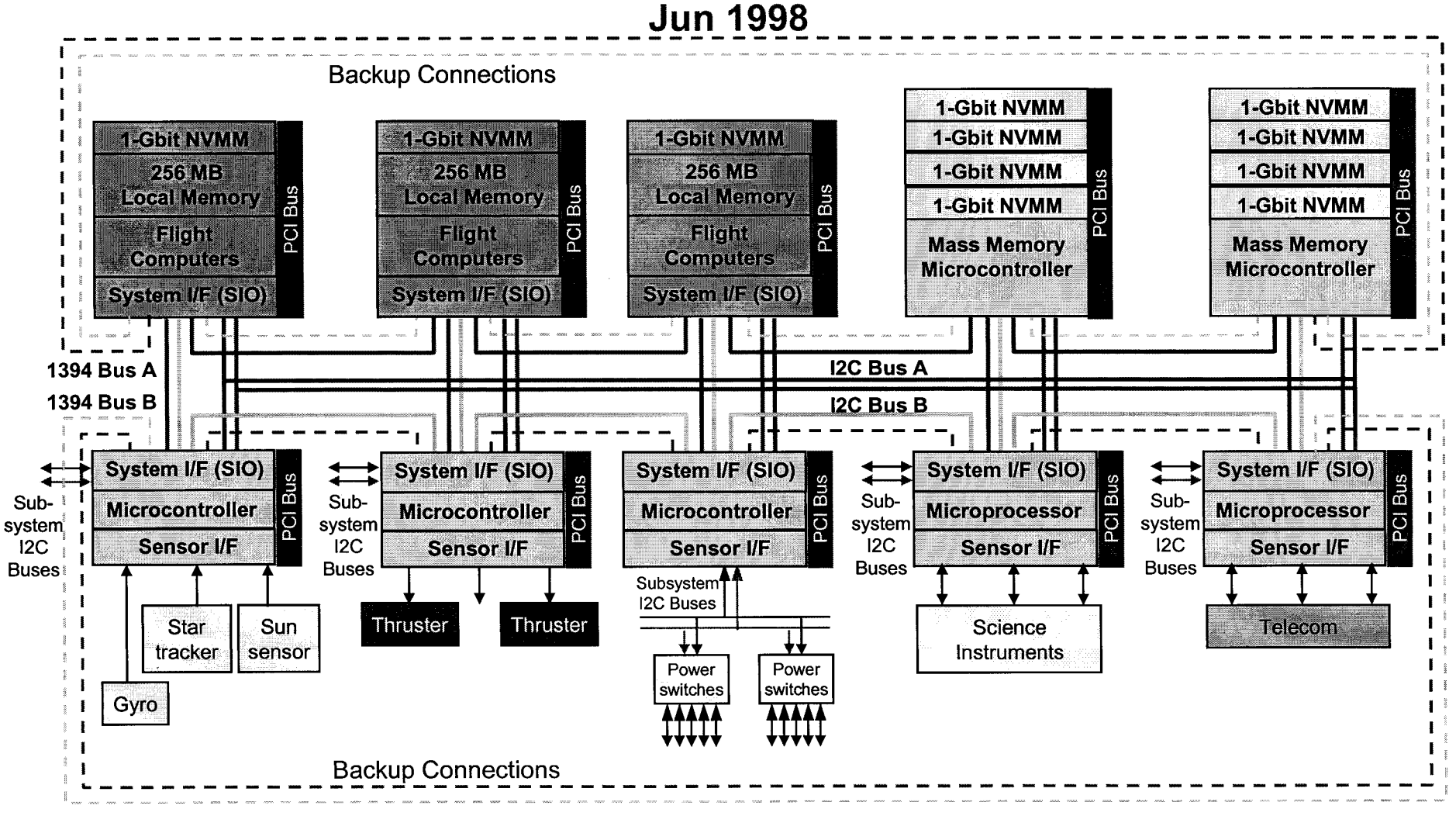
  The 1394a spec has a port disable feature. When a port is disabled, it is invisible. This feature can be used to implement alternative topologies in the same tree. Faults can be tolerated include stuck-at, short, babbling nodes etc.



Multiple failures can be tolerated by this approach. Example:



Revised X2000 Baseline Avionics Architecture

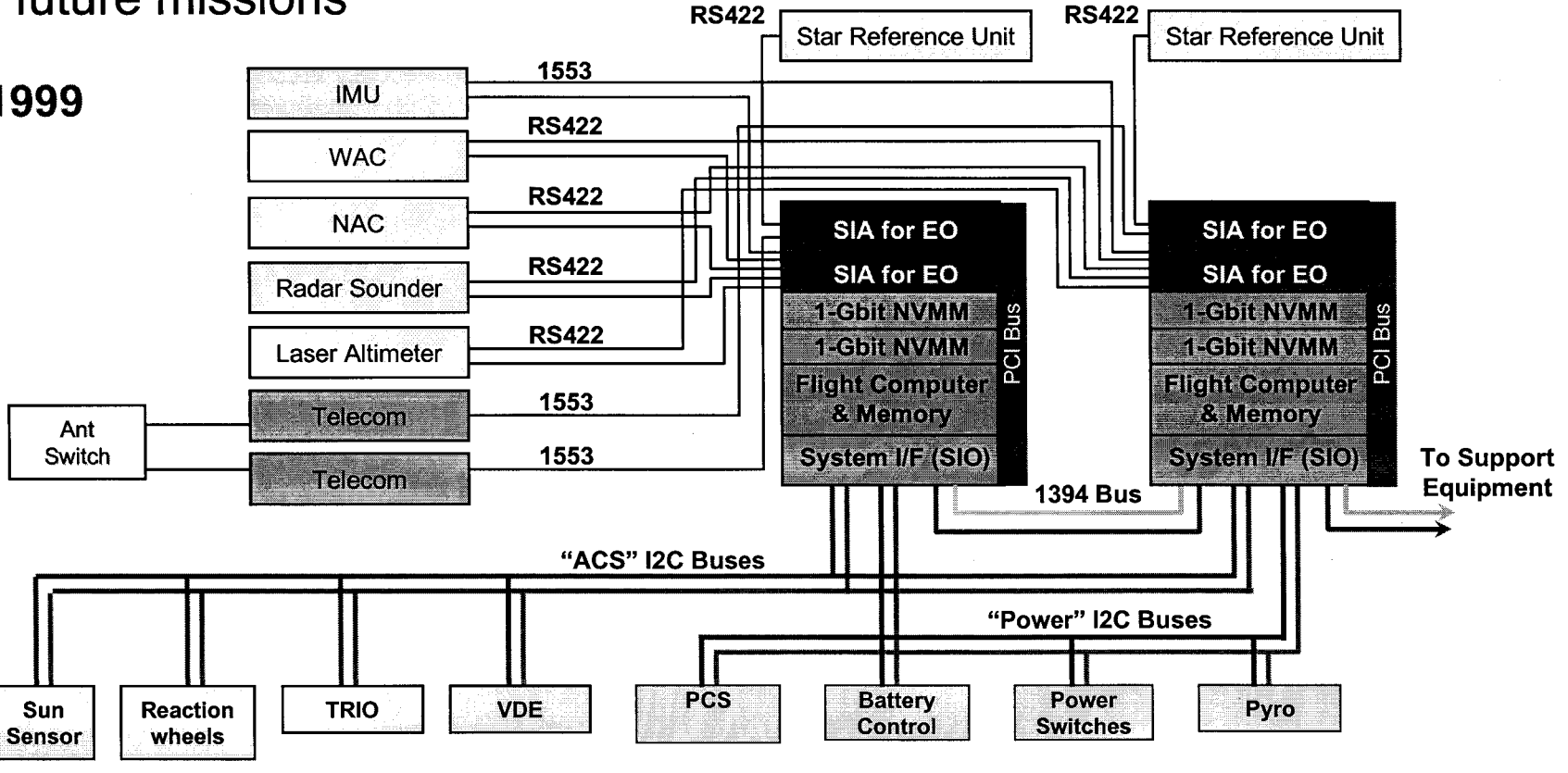


Note: A multi-level fault protection approach was also developed as a result of the tiger team review (to be presented)

X2000 Architecture Descope Due to Funding

- Microcontroller development was descoped due to funding constraint. Distributed architecture is no longer baseline
- IEEE 1394 and I2C bus development are continued to allow expansion by future missions

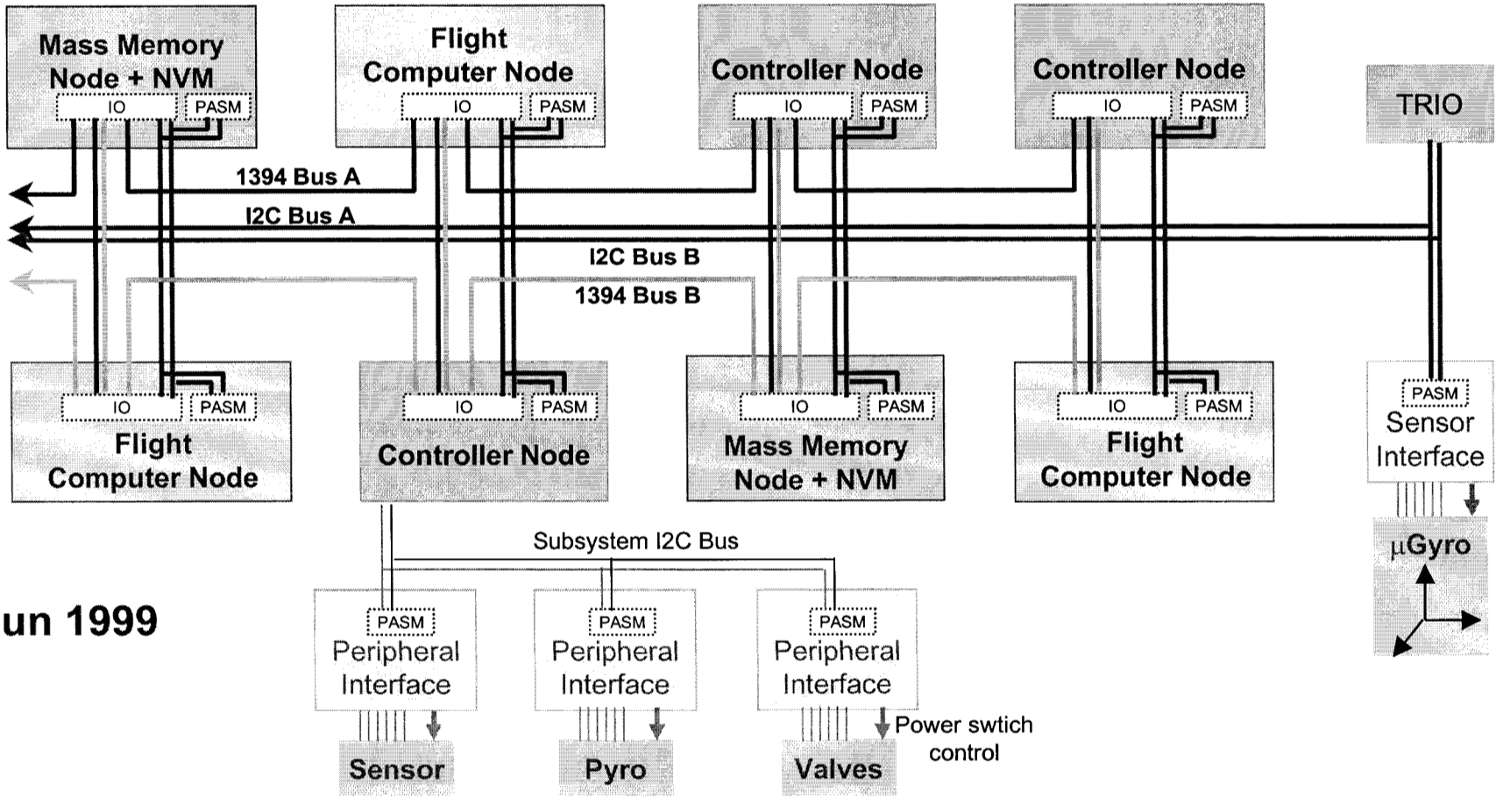
Sep 1999



X2000 Avionics System to be Delivered to Europa Orbiter

X2000 Future Deliveries

- IEEE 1394 and I2C based
- All circuits in a node is contained in a single module. No PCI outlet
- Distributed power switching through I2C bus



Jun 1999

Summary and Conclusion

- Presented the X2000 avionics system bus selection process
- Presented the evolution of the X2000 avionics system
- The IEEE 1394 and I2C buses have been preserved throughout the evolutions and being implemented for the Europa Orbiter mission
- The development of IEEE 1394 and I2C buses will continue at JPL

Implementation of Fault Tolerant IEEE 1394 Bus Architecture in X2000

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X2000 Bus Requirement

- X2000 system bus major requirements
  - Advanced technology
  - Multi-mission: scalable, distributed, and symmetric
  - Low cost
  - High performance: Original Europa Orbiter bandwidth > 40 Mbps
  - Low power, mass, and volume
  - Reliable and fault tolerant
- It was decided that commercial bus standards can meet the first five criteria better than space qualified buses (e.g. 1553). The last criterion can be addressed by system level design.

Note: Despite the relaxation of some of the requirements, due to funding and schedule constraints, the X2000 architecture is still capable of supporting all of these requirements

Bus Selection Summary

	1st Round Selection	2nd Round Selection
IEEE 1394	✓Very good data rate, moderate power, strong commercial support, relatively deterministic latency, no rad-hard parts but ASIC core available, although weak in fault-tolerance	✓Power is moderate and data rate is appropriate, tree topology can be fitted into the MCM stack by using linear tree, fault protection can be achieved by mirroring the linear tree
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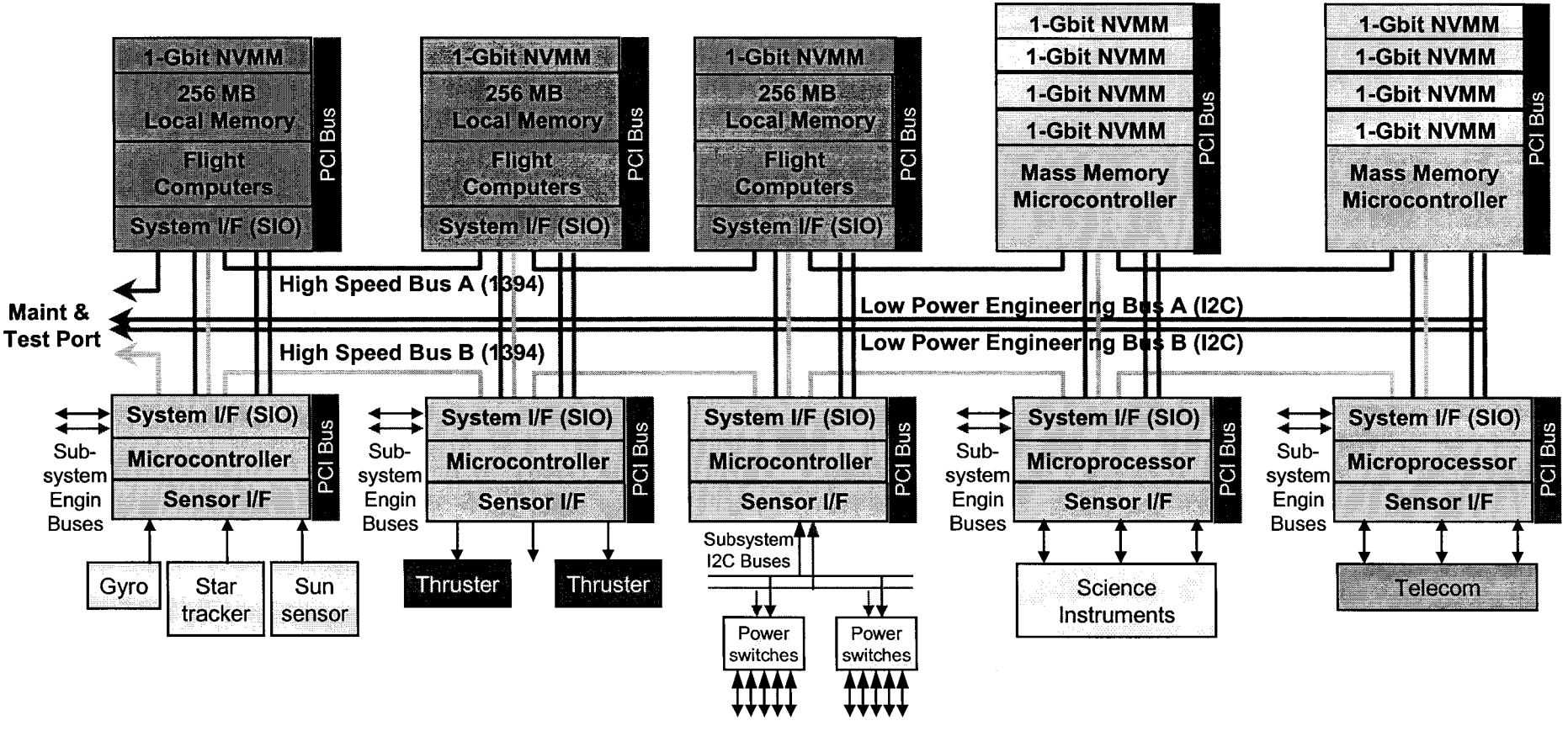
Original Baseline X2000 Avionics Architecture



Note: The X2000 avionics architecture has been descoped due to funding and schedule constraints. However, the IEEE 1394 and I2C buses are preserved to support scalabilty for future missions

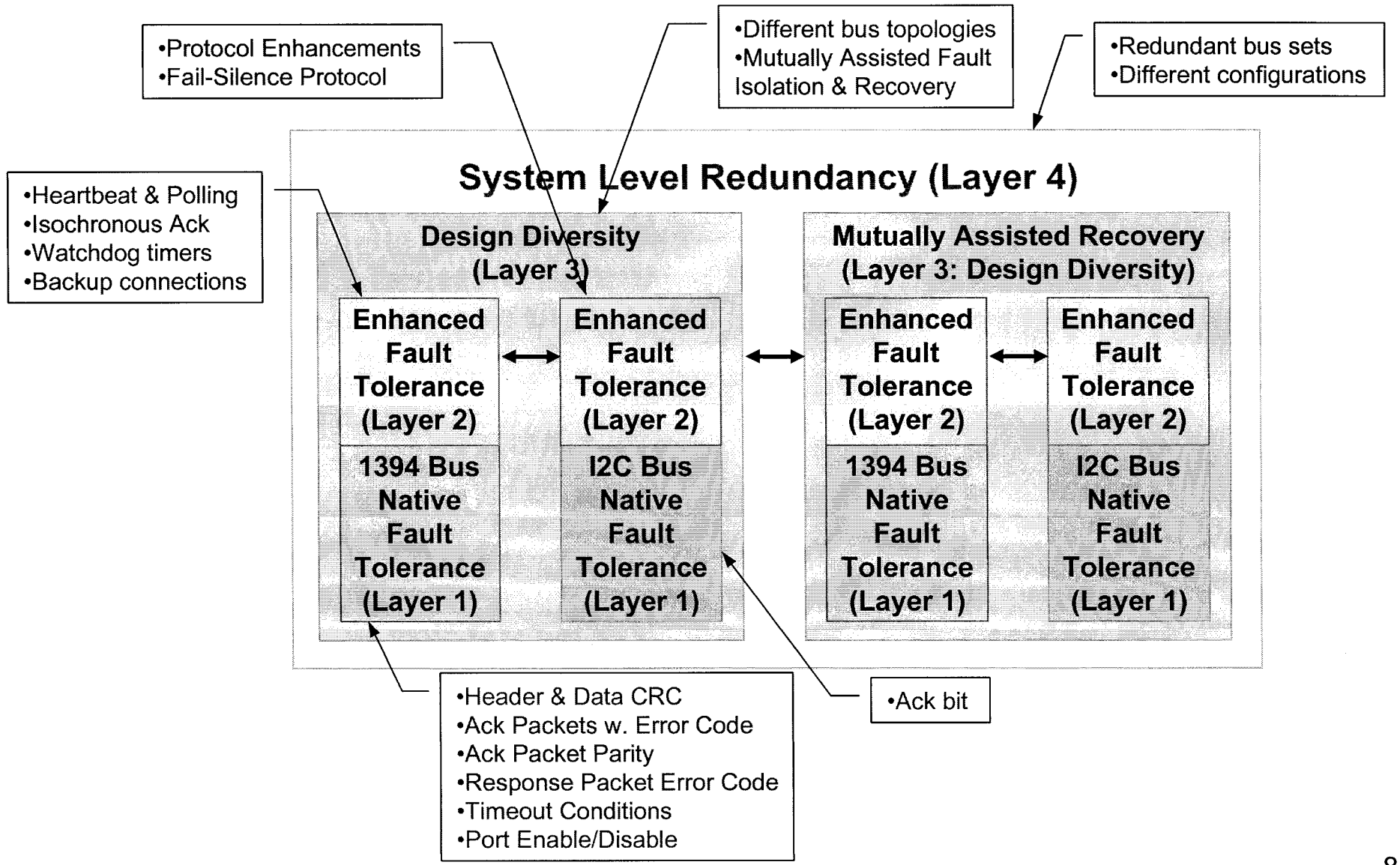
Challenges of Using IEEE 1394 for Deep Space

- Space qualified parts are not available. Commercial components do not meet space environmental requirements
- The IEEE 1394 standard has relatively good fault detection but insufficient mechanisms for effective fault recovery
- Design techniques of commercial parts might not be suitable for space applications. For example, dynamic logic such as pre-charge circuits are not suitable for high radiation environments
- Commercial vendors will not change their designs for a "narrow" market of reliable computing

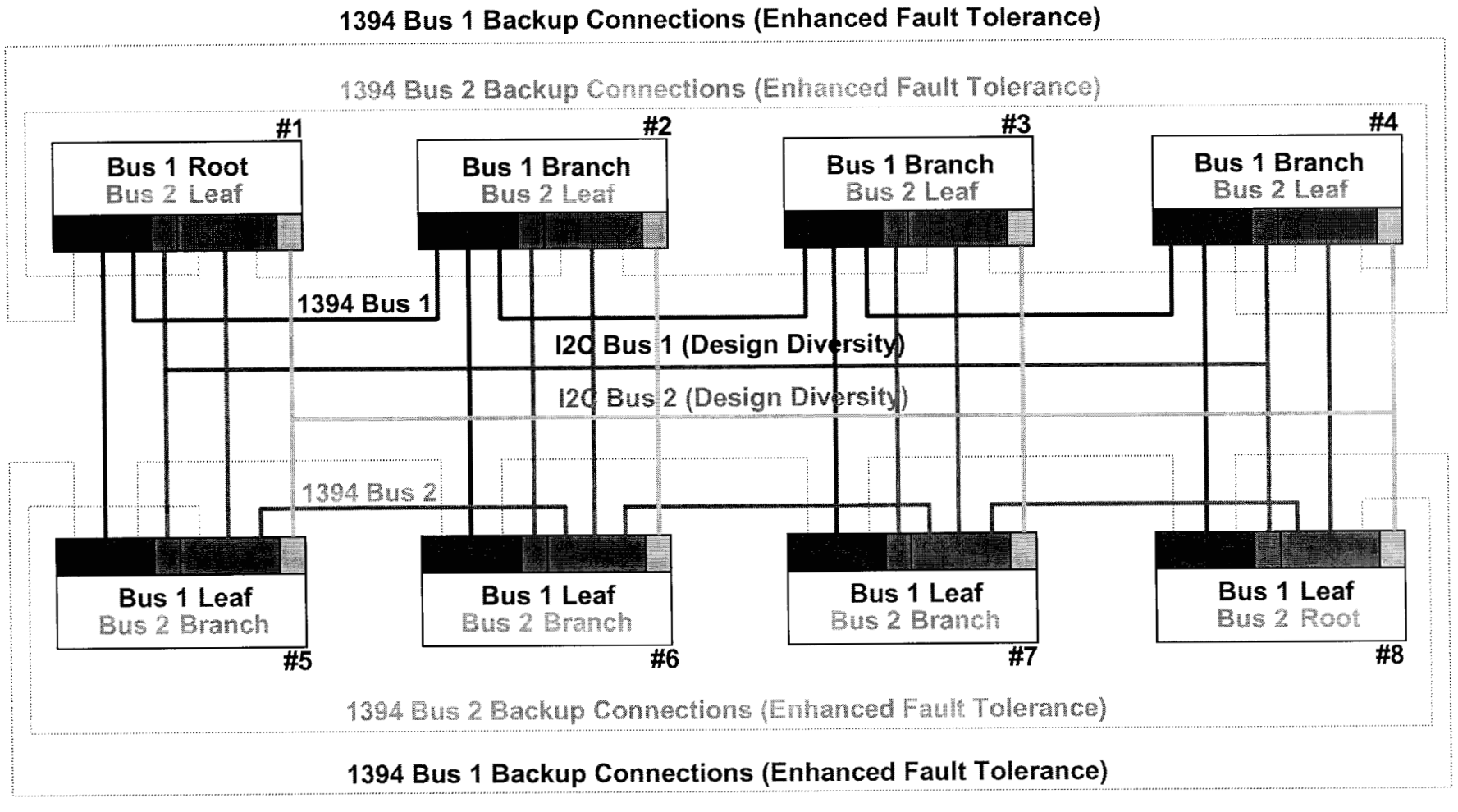
X2000's Approach to Adopt IEEE 1394

- Develop IEEE 1394 parts using COTS Intellectual Properties (IP) and fabricate the parts on a rad-hard foundry. The parts being developed are
  - IEEE 1394 Link Layer to PCI ASIC
    - COTS IEEE 1394 Link Layer IP
    - COTS PCI IP
    - COTS I^2C IP
    - COTS UART IP
    - Custom designed miscellaneous logic
  - IEEE 1394 Physical Layer ASIC
    - COTS IEEE 1394 Physical Layer digital IP
    - Custom designed analog circuits for IEEE 1394 Physical Layer and I^2C
- Develop a multi-level approach to enhance the fault tolerance of the IEEE 1394 bus

Multi-Layer Fault Tolerance Methodology

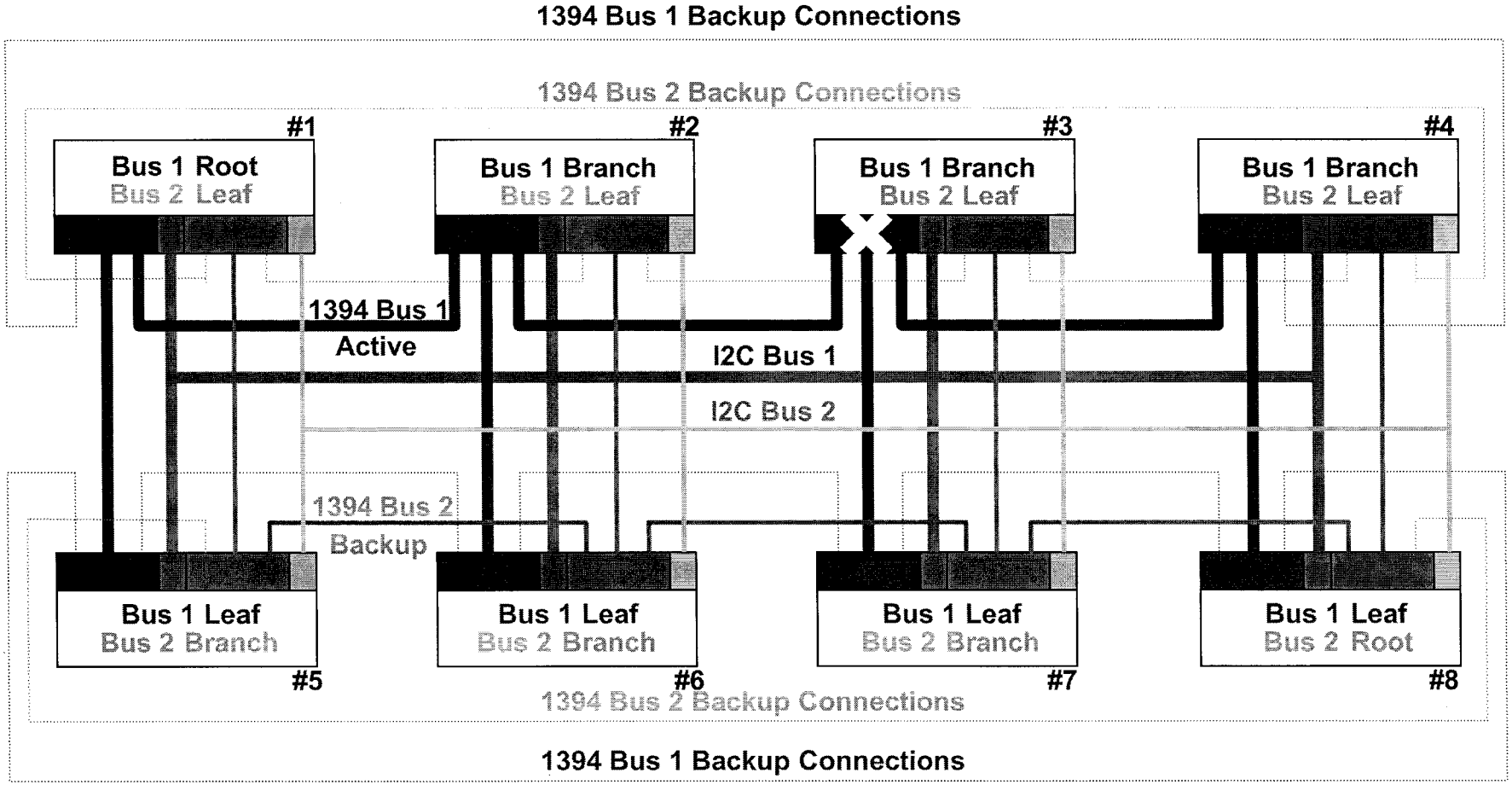


Realization of Multi-Level Fault Protection



System Level Redundancy with Different Configuration

Example of Fault Recovery



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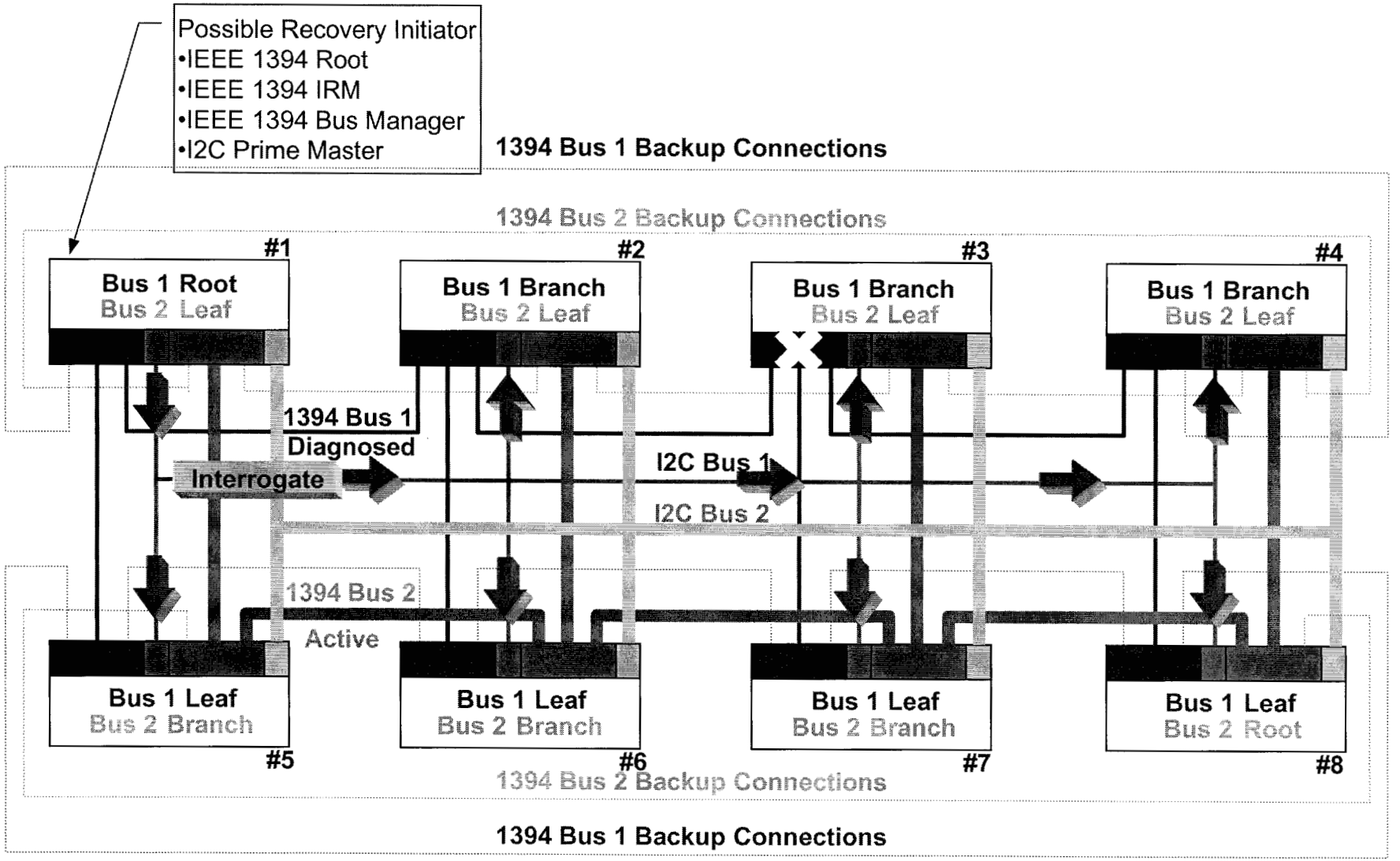

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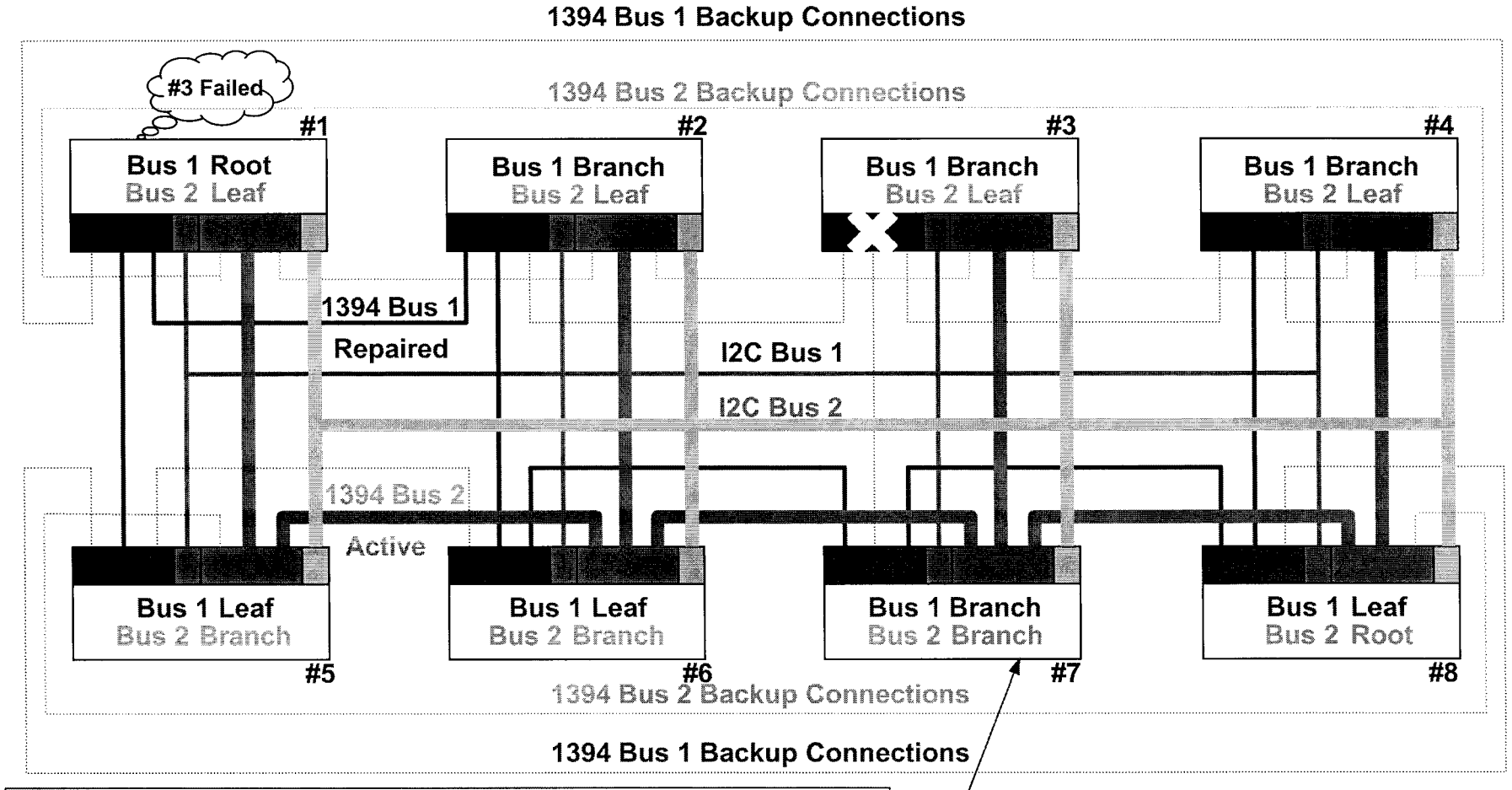
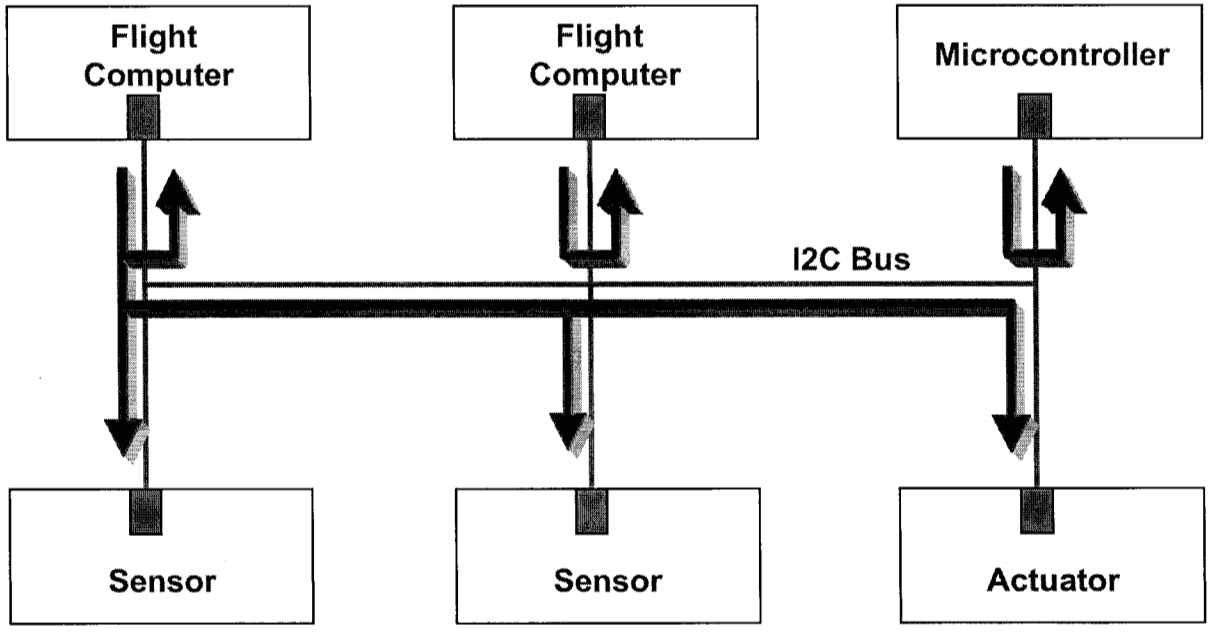


I2C Bus Fault Protection: Fail Silence



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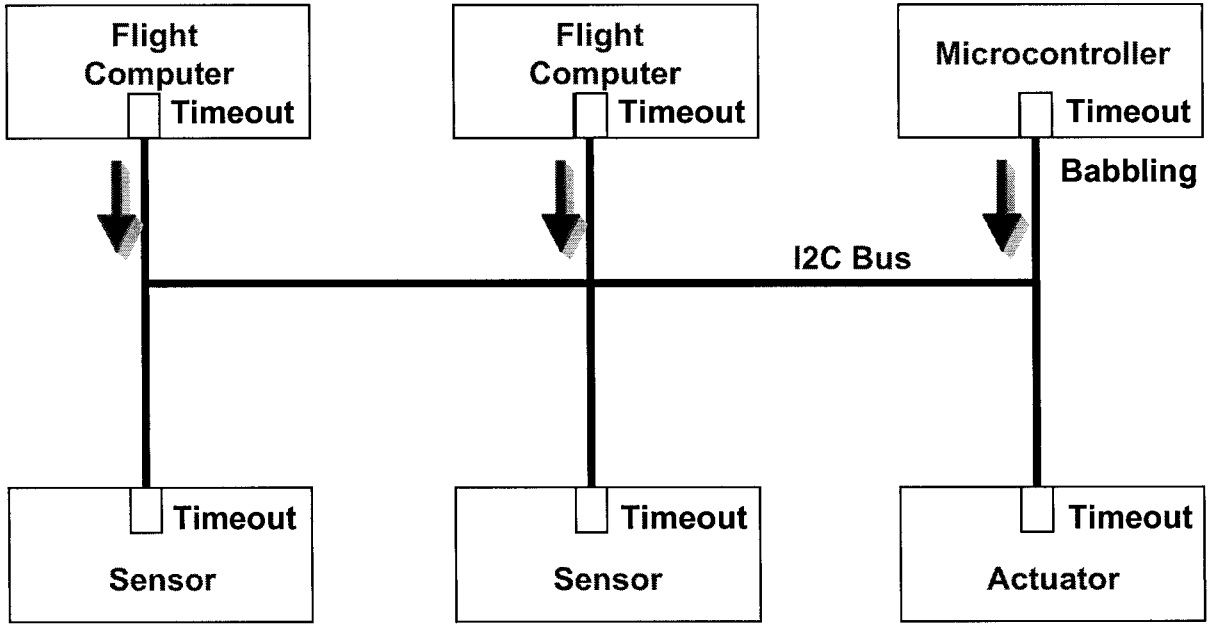

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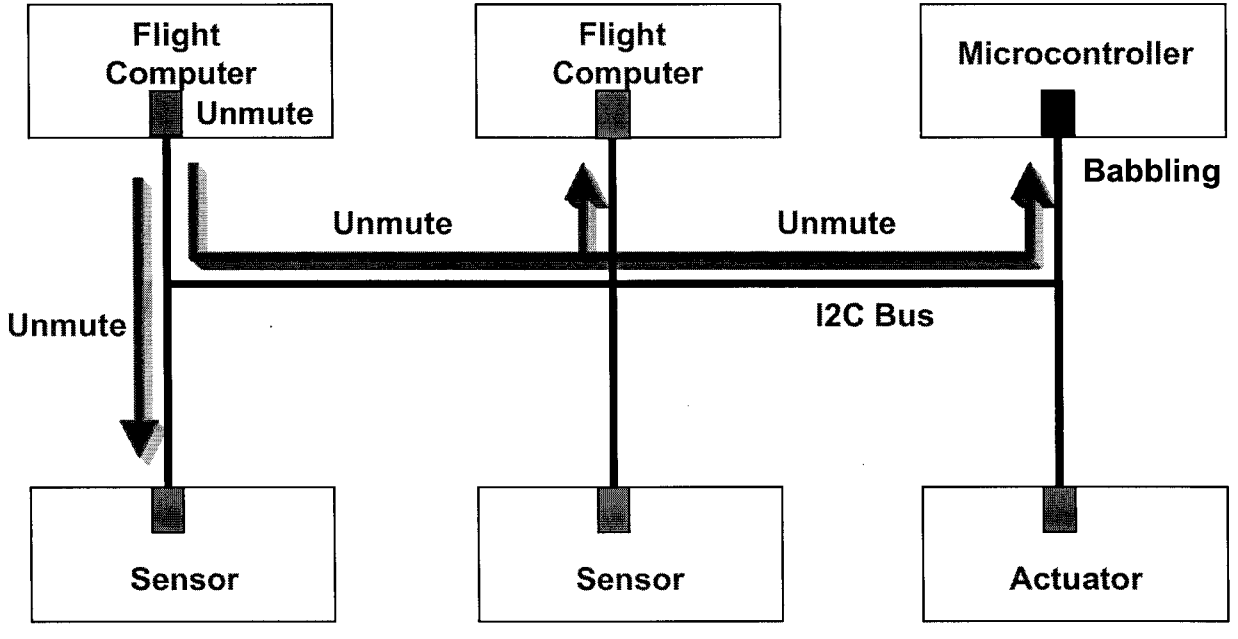
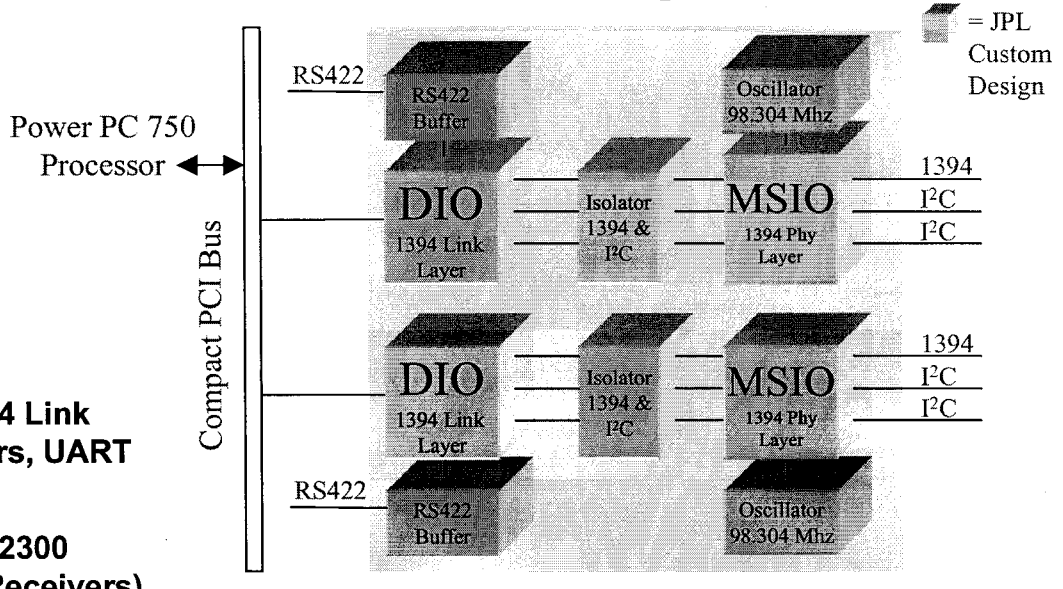


I2C Failure Mode Effects Containment Analysis completed 2/00

SIO Board Overview

- **Function: Interface between 7 Buses**
  - 1@ Compact PCI bus (PICMG 2.0 R2.1)
  - 2@ IEEE 1394a Bus - 100 Mbps
  - 4@ I^2C Bus - 100 Kbps
- **Specifications**
  - TID > 1 Mrad
  - SEU > 1E-10 Errors/Bit-Day (GCR env.)
  - DIO: Gate Array, Honeywell HX3800 (1394 Link Layer, I/F to cPCI Bus, I^2C Bus Controllers, UART 16550, and Custom Logic)
  - MSIO: Mixed Signal ASIC, Honeywell HX2300 (1394 Phy Layer , I^2C and 1394 Drivers/ Receivers)
  - Isolation: Full Galvanic Isolation Between PCI and the 6 serial buses via Transformers and multiple gnd regions of MSIO
  - Power: 1 Watt Est. in High Power Mode
  - Mass: 0.4 Kg Est.

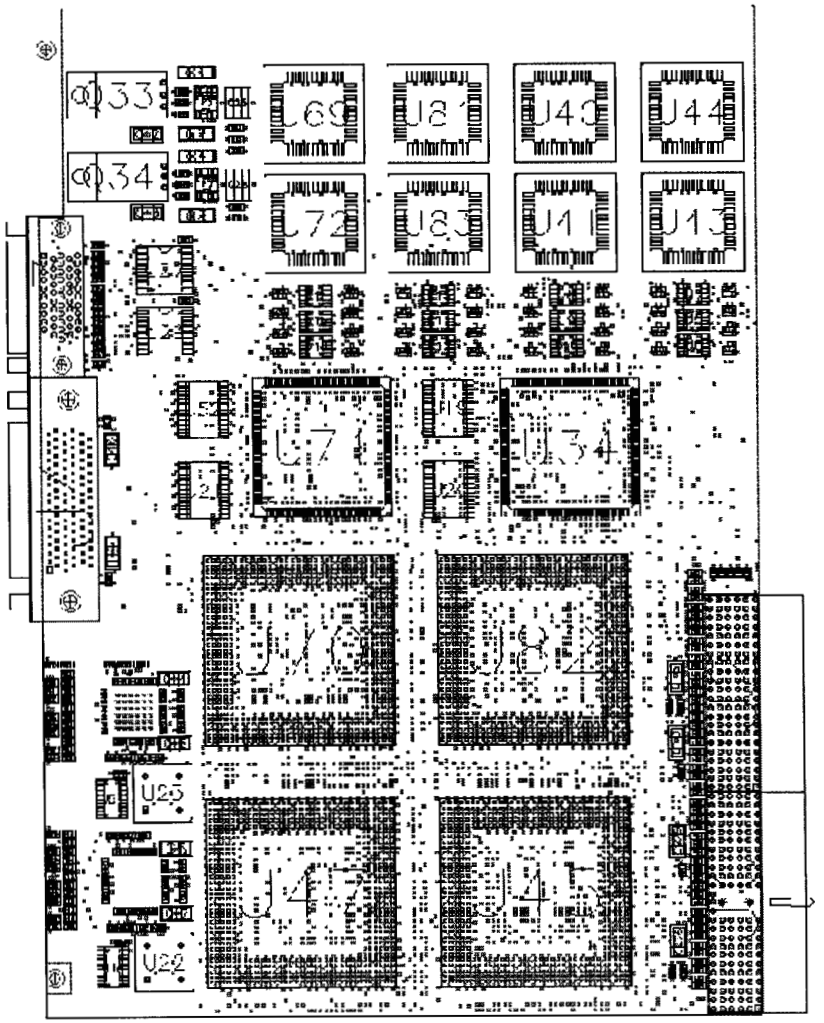
Block Diagram



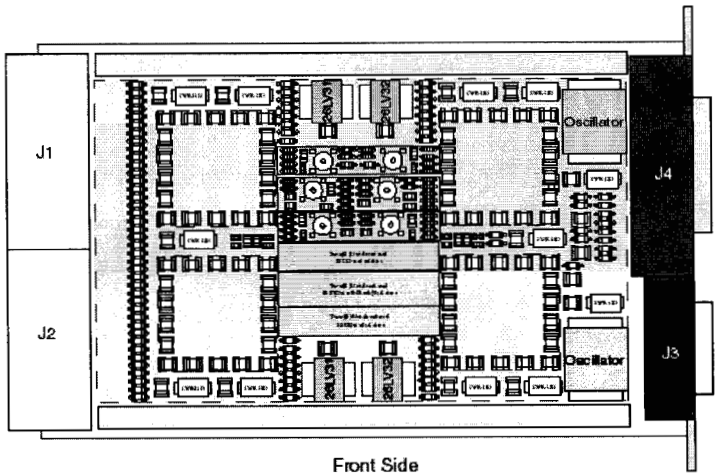
- **Commercialization Plans**
  - –Commercial Vendor FY01-02
  - –RE target EM $100K, FM $150K

SIO Mechanical Overview

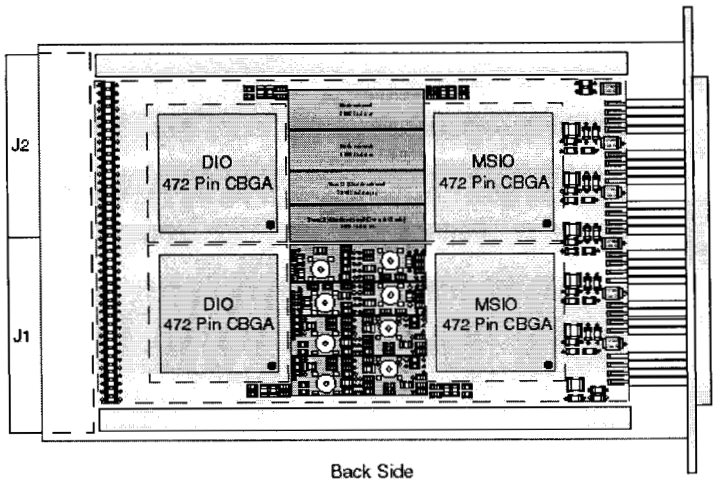
Prototype (Q1/00)
6U CPCI



Engineering Model (Q4/00)
3U CPCI



Front Side



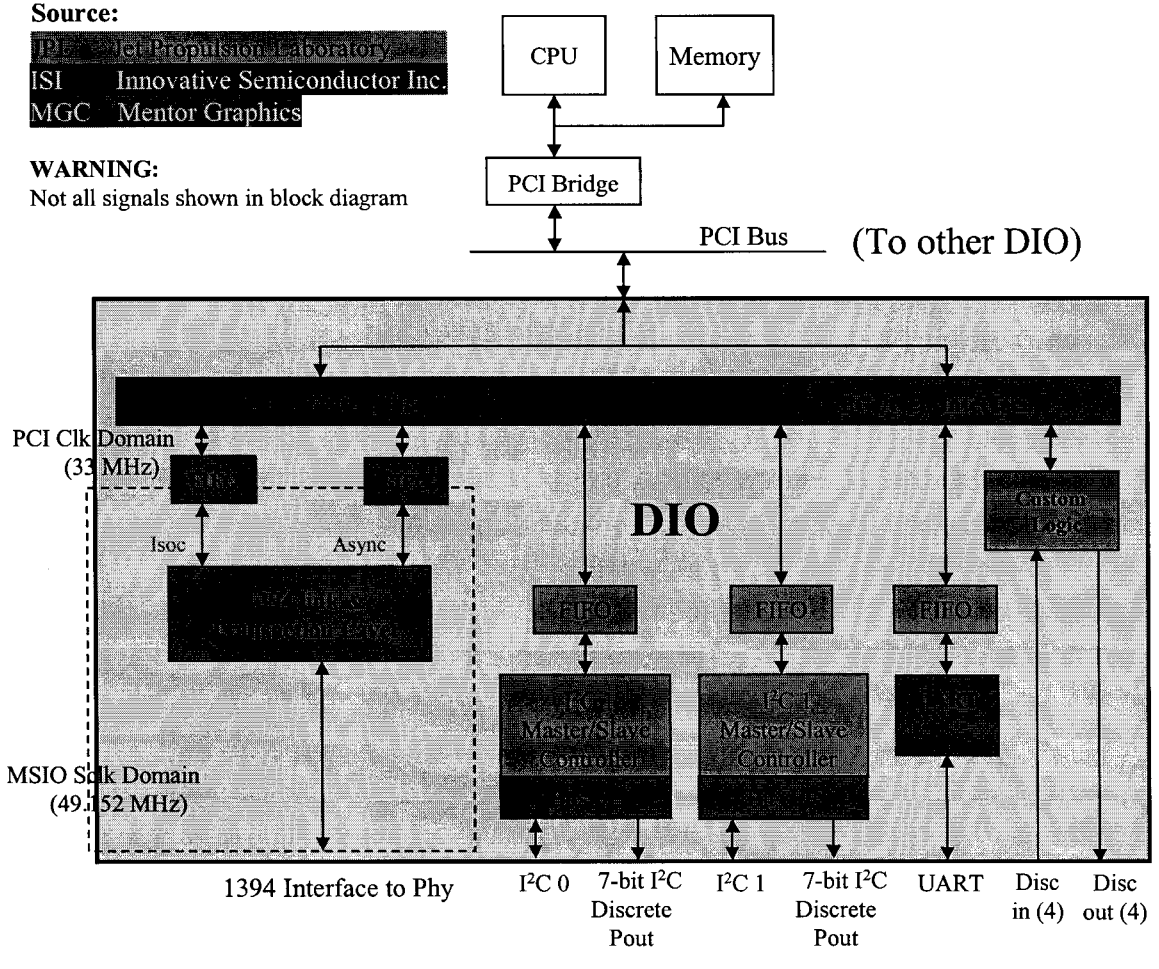
Back Side

Digital I/O (DIO) ASIC overview

Source:

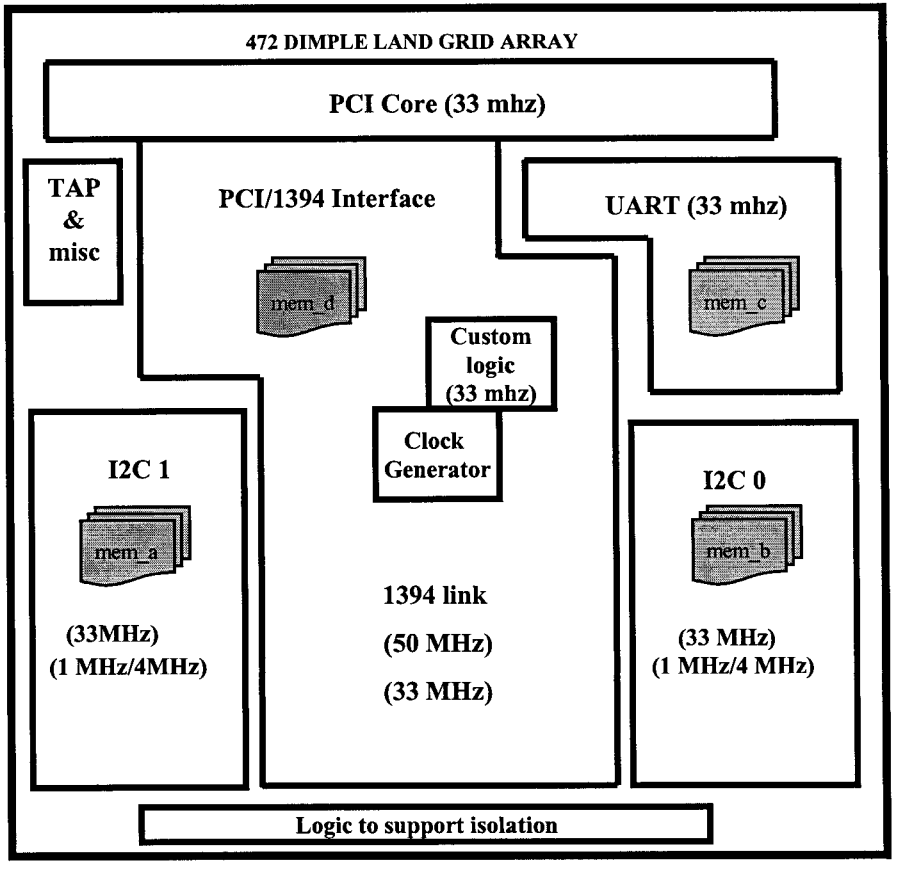
JPL Jet Propulsion Laboratory
ISI Innovative Semiconductor Inc.
MGC Mentor Graphics

WARNING:
Not all signals shown in block diagram



- Functionality::
  - * Link & Transaction Layer of 1394 Protocol (100-400Mbps)
  - * 2 I²C interfaces containing high reliability protocol controller
  - * 16550 UART
  - * custom logic fault protection circuitry
  - * PCI I/F (Initator for 1394, Target for I2C, Uart, Custom Logic. Zero wait state transfers)
- Design Team:
  - * JPL (Specification, I²C I/F, Custom logic, overall integration, simulation, synthesis)
  - * Innovative Semiconductors, Inc. (Link and Transaction IP)
  - * Mentor Graphics (PCI,UART,I2C IP)
  - * Honeywell (Layout and Fabrication)
- Specifications:
  - * Pototype
    - * Xilinx XCV800 FPGAs (2) + SRAM
    - * 1/2 speed CPCI, 1/4 speed 1394
  - * EM/FM
    - * HX3800, 3.3V Gate Array, 0.35uM
    - * 472 pin BGA package
- * Development Status
  - * PT Debug started 11/99, 50% done
  - * ASIC PDR 5/00

DIO ASIC Floor Plan



HX3800
790K Gates
533 x 478 mils
0.35µm, Silicon-on-Insulator (SOI) Technology
Gate Array with/Embedded SRAM

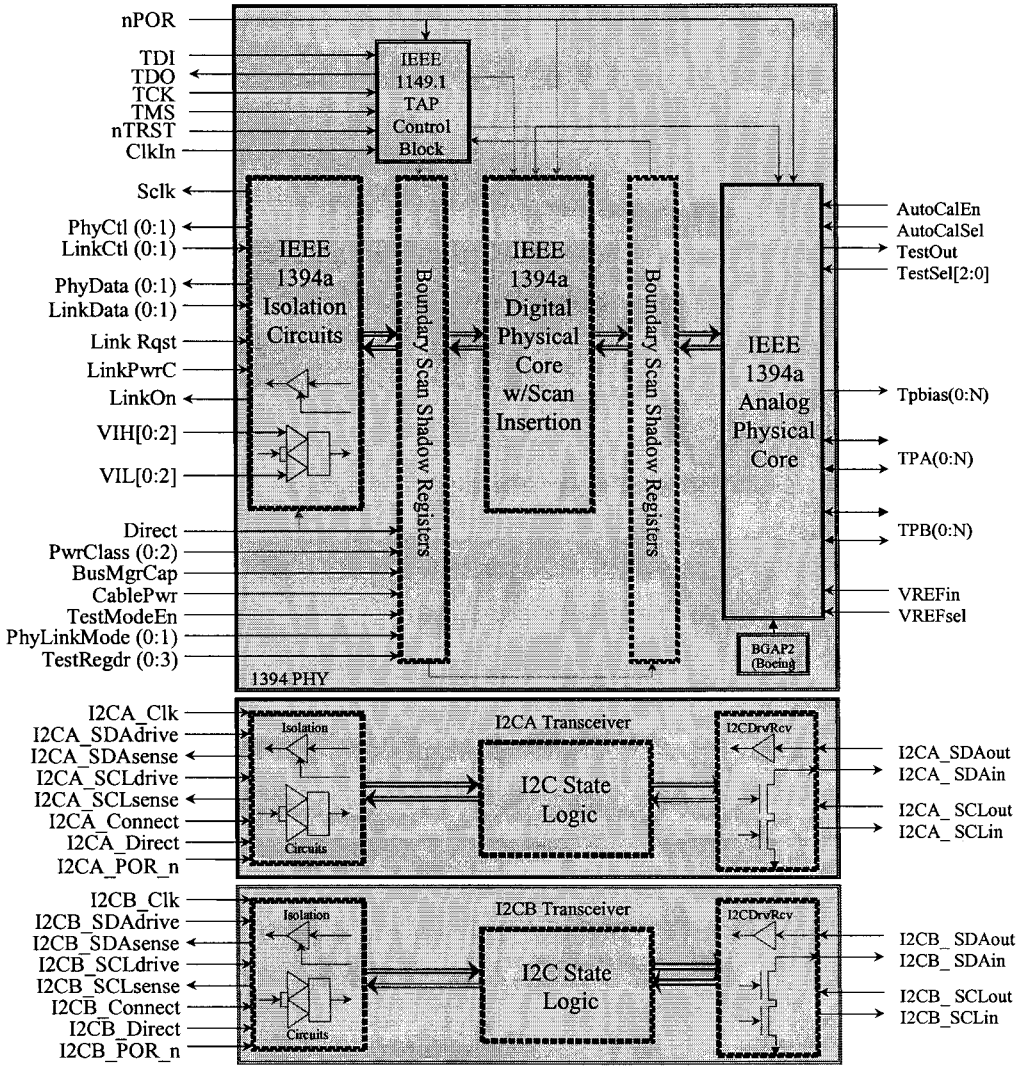
Memory Sizes

mem_a : Custom RAM 128 x 32 (4)
mem_b : Custom RAM 128 x 32 (4)
mem_c : Custom RAM 128 x 32 (2)
128 x 8 (1)
mem_d : Custom RAM 8 k x 36 (1)

Post-scan cell count (approx)

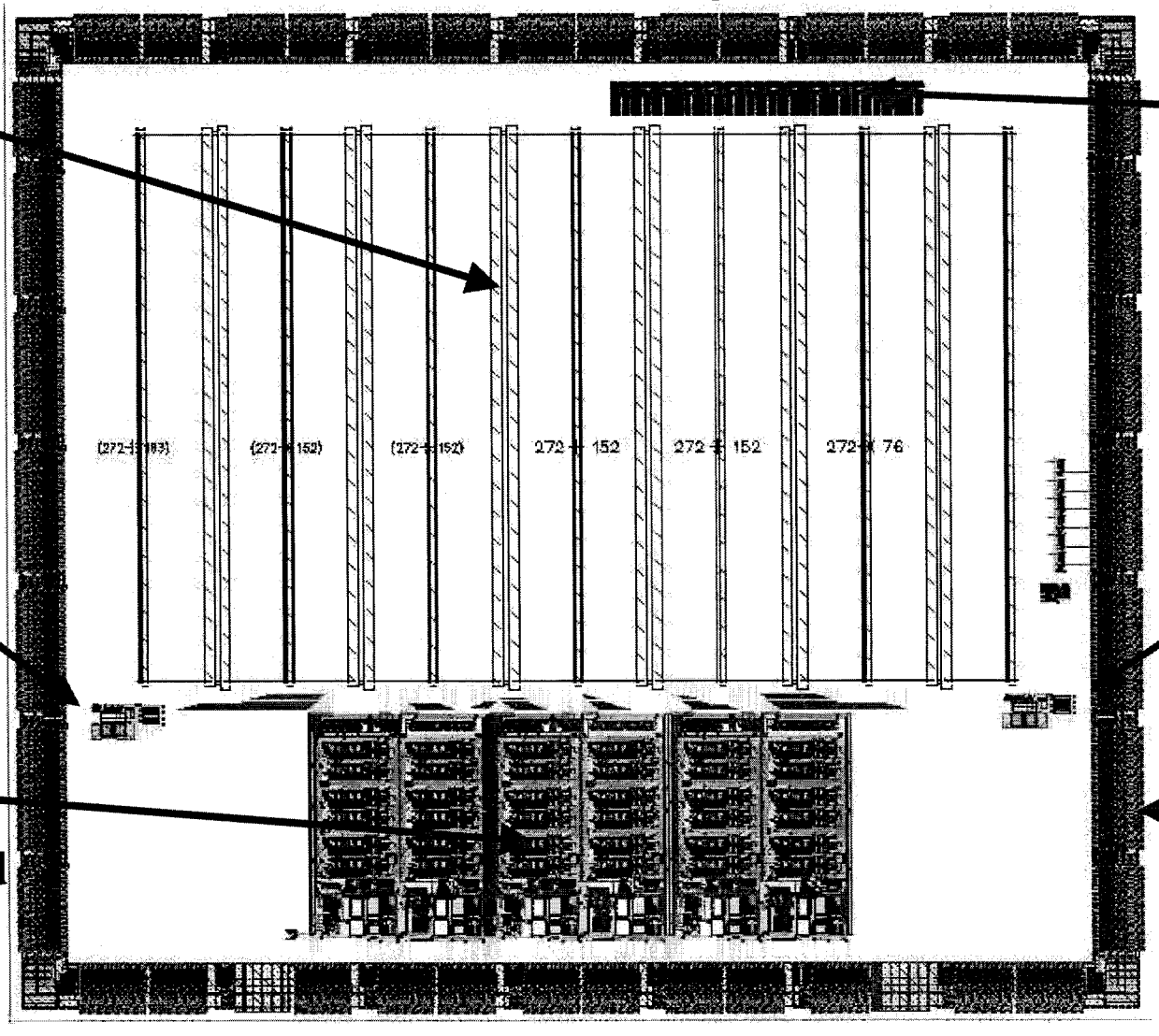
	Combin.	Sequen.	Total	Accum.
UART	13,747	44,488	58,235	58,235
I2C 0	21,304	80,676	101,980	160,215
I2C 1	21,304	80,676	101,980	262,195
1394 Link	41,590	49,375	85,965	348,160
custom	4,845	7,602	12,447	360,607
clk_gen	977	2,044	3,021	363,628
iso	67	308	375	364,003
tpmux	63	0	63	364,066
io cells	10,602	0	10,602	374,668
bsr	2,350	6,292	8,642	383,310
tap	79	200	279	383,589
PCI core	9,654	12,196	21,850	405,377
PCI/1394/ram		266,418	266,418	671,795

MSIO ASIC overview



- **Functionality:**
  - 1@ 1394 S100 Physical Layer (98.304 Mbps)
  - 2@ I²C physical interfaces
    - slew-rate limited drivers
  - 3@ separate power domains
    - isolated WRT DIO & each other
- **Design Team:**
  - JPL (Specification, overall integration, simulation, analysis)
  - Innovative Semiconductors, Inc. (Digital 1394 Phy block)
  - Boeing (Voltage Reference)
  - Honeywell (Layout)
  - Digital Media Com (Analog Physical layer, I2C blocks)
- **Specifications:**
  - Prototype
    - **COTS TI TSB41LV03 + misc. parts**
  - EM/FM
    - **HX2300r mixed signal**
    - **0.7uM SOI CMOS**
    - **472 pin BGA package**
- * **Development Status**
  - * Analog Phy Prototype ASIC rad tested 10/99
  - * ASIC PDR 5/00

MSIO ASIC layout



HX2300R - 533x478 mils - Mixed Signal - 0.7uM Silicon-on-Insulator (SOI)

Summary and Future Work

- IEEE 1394 was selected by X2000 because it can meet the scalability, performance, cost, and power requirement
- The weakness of IEEE 1394 in fault tolerance is compensated by a multi-level fault tolerance methodology
- COTS IPs are used to implement the ASICs required by the multi-level fault tolerance methodology
- Hardware implementation of the COTS-based multi-level fault tolerance X2000 system is being developed
- The hardware and software described will be the basis of the upcoming Europa Orbiter and Pluto/Kuiper Express missions
- **A truly fault tolerant IEEE 1394 bus should be developed for space applications**